60V, 0.6A, 1.6MHz, Synchronous, Step-Down Converter

Description

The ME3136 is a wide-Vin, easy-to-use synchronous buck converter capable of driving up to 0.6A load current. The ME3136 employs fixed-frequency peak-current mode control for fast loop response. With a wide input range of 4.5V to 60V, the device is suitable for a wide range of industrial applications for power conditioning from an unregulated source.

The 1μA shutdown mode quiescent current allows the device to be used in battery-powered applications. The ME3136 uses high duty cycle and low dropout mode for low input voltage conditions.

The ME3136 operates at 1.6MHz switching frequency to support use of relatively small inductors for an optimized solution size.

The ME3136 has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, and thermal shutdown in case of excessive power dissipation. Soft-start and compensation circuits are implemented internally, which allow the device to be used with minimal external components.

The ME3136 is available in a cost-effective SOT23-6 package.

Feature

- Meets 0.1% output voltage ripple
- 4.5V to 60V operating input range
- Withstands up to 65V short VIN transient
- 2%-98% large range duty cycle
- Wide range of frequency foldback
- >90% efficiency
- Precision enable
- Dedicated internal compensation
- Stable with ceramic/electrolytic output capacitors
- 420mΩ/220mΩ internal power MOSFETs
- 1.6MHz fixed switching frequency
- Internal soft start (SS) with pre-biased output
- Precision current limit
- Hiccup mode short-circuit protection
- Output adjustable from 0.8V to 0.95xVIN
- Over temperature protection
- Available in a SOT23-6 package

Applications

- Power meters
- Aftermarket automotive
- PLC, DCS, and PAC
- General purpose wide VIN power supplies

Package

- 6-pin SOT23-6

Typical Application Circuit

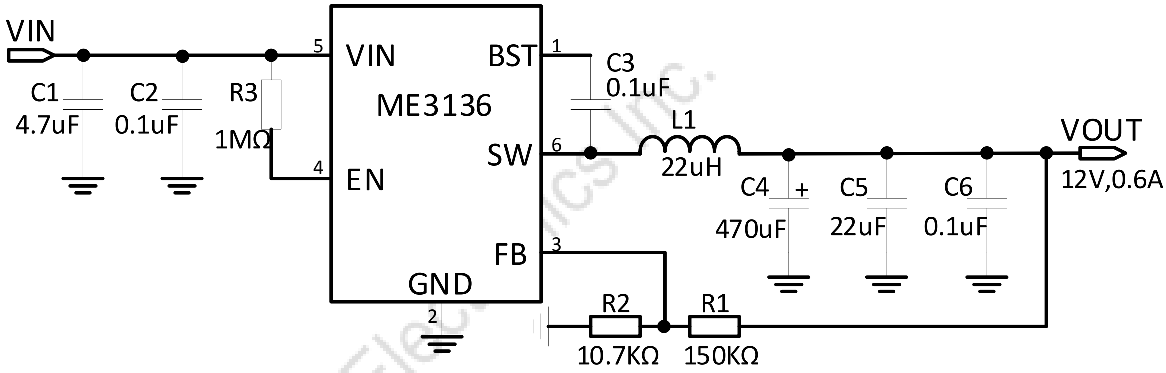


Figure1. 12V Output

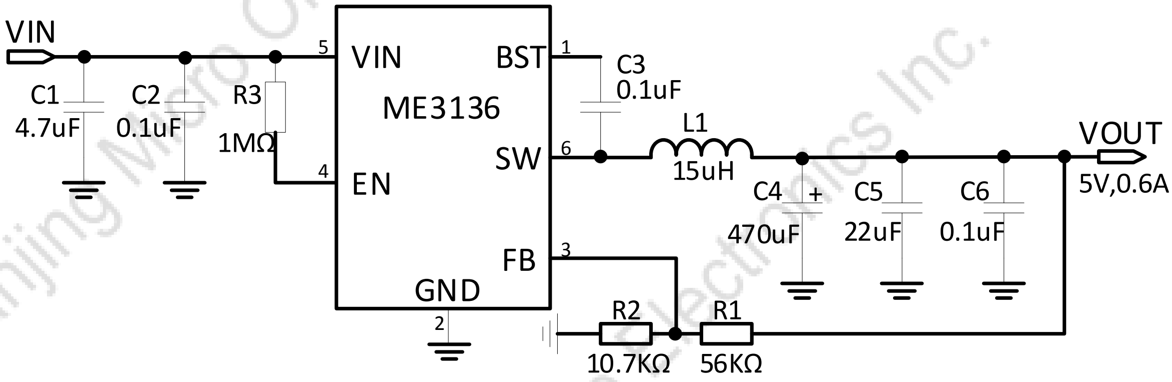


Figure2. 5V Output

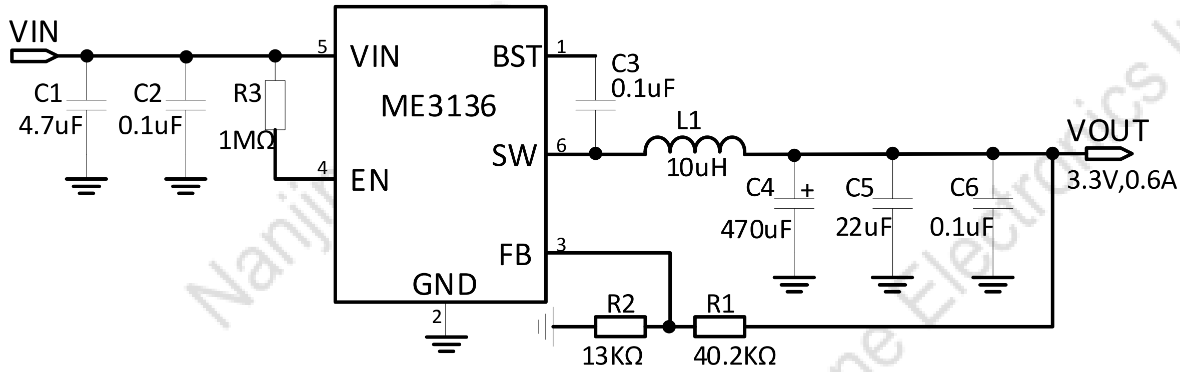
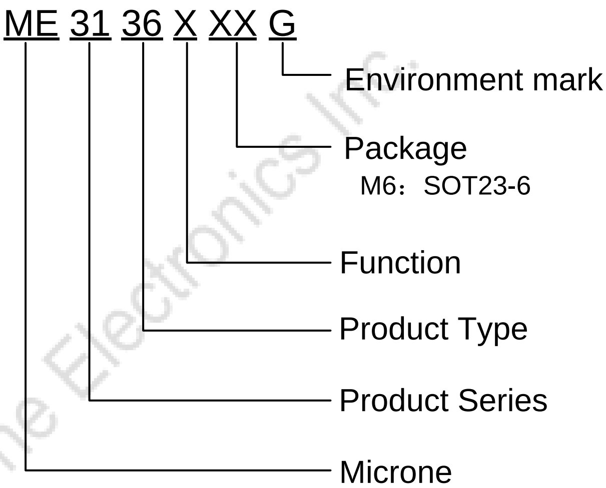


Figure3. 3.3V Output

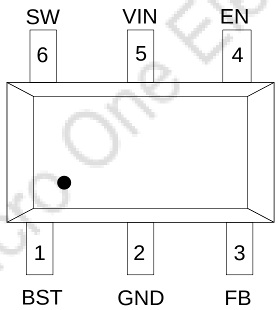
Selection Guide



product series	product description
ME3136AM6G	package: SOT23-6

NOTE: If you need other voltage and package, please contact our sales staff。

Pin Configuration

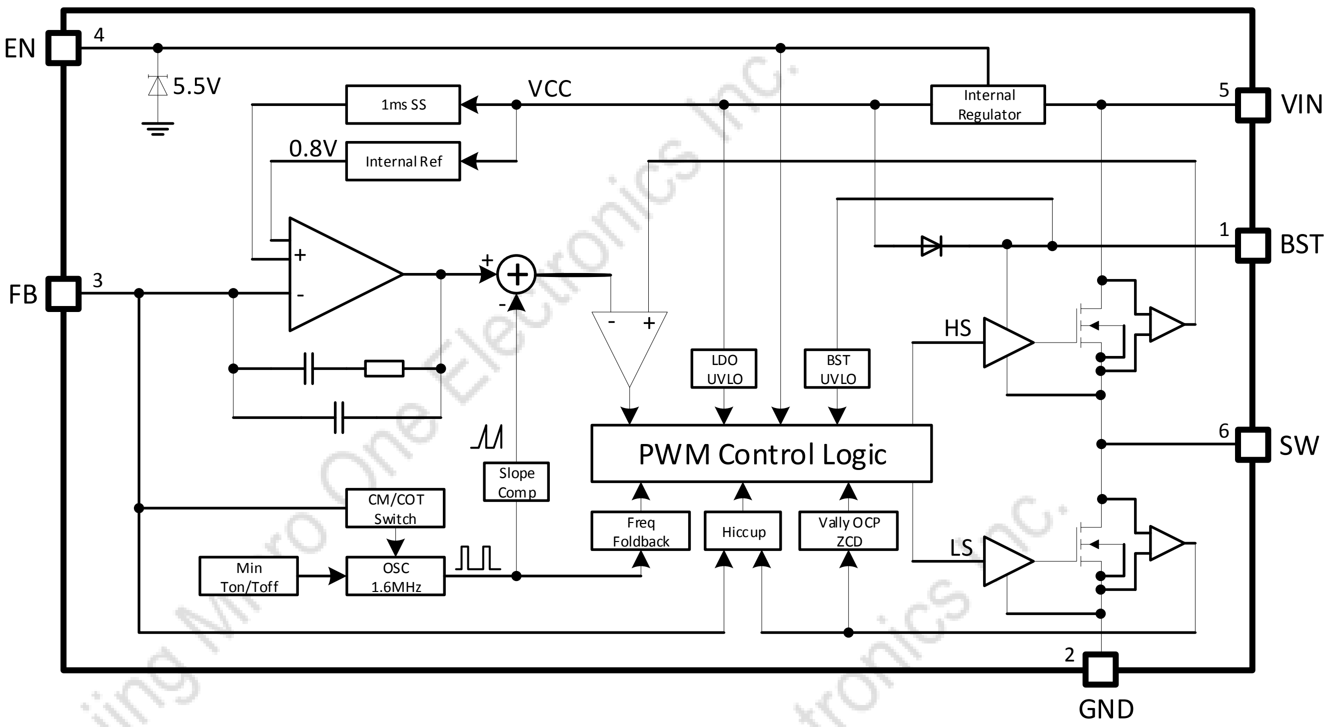


SOT23-6

Pin Assignment

PIN Number	symbol	Function
1	BST	Bootstrap capacitor connection for high-side FET driver. Connect a high quality 100-nF capacitor from this pin to the SW pin.
2	GND	Ground. Connect an output capacitor as close to GND as possible. Avoid routing GND near high-current switch paths.
3	FB	Feedback. Feedback input to the converter. Connect a resistor divider to set the output voltage. Never short this terminal to ground during operation.
4	EN	Enable input. Pull EN below the specified threshold to shut the chip down. Pull EN above the specified threshold to enable the chip. Float EN to disable the chip.
5	VIN	Input supply. Supply input pin to the internal bias LDO and high-side FET. Connect to the input supply and input bypass capacitors. Input bypass capacitors must be directly connected to this pin and GND.
6-	SW	Switch node. Internally connected to source of the high-side FET and drain of the low-side FET. Connect to the power inductor.

Block Diagram



Absolute Maximum Ratings

Parameter		Symbol	Ratings	Units
Supply voltage		V_{IN}	66	V
Switch voltage		V_{SW}	0.3~ V_{IN}+3	V
BST to SW			6	V
All other pins			6	V
Continuous power dissipation (T_A=25°C)[2]	SOT23-6	Pd	400	mW
Package thermal resistance (θ_{JA})	SOT23-6	θ_{JA}	200	℃/W
Package thermal resistance (θ_{JC})	SOT23-6	θ_{JC}	100	℃/W
Storage Temperature Range		T_{stg}	-65~+150	℃
Maximum junction temperature		T_J	150	℃
Lead temperature & time			260°C, 10S	
ESD (HBM)			2000	V

Notes:

1) Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product.

2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_{J\,(MAX)}$, the junction-to- ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D(MAX)}=(T_{J(MAX)}-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Recommended work conditions

Item	Min	Recommended	Max.	Unit
Supply voltage (V_{IN})	4.5		60	V
Output voltage (V_{OUT})	0.8			V
Operating junction temp (T_J)	-40		85	°C

Electrical Characteristic

V_{IN}=12V, V_{EN}=2V, T_J=-40°C to +125°C [4], unless otherwise noted. Typical values at T_J=+25°C..

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Feedback voltage	V_{FB}			0.8		V
Feedback bias current		V_{EN}=1V, V_{FB}=2V			0.1	μA
High-side switch on resistance[3]	R_{ON_HS}	V_{BST}-V_{SW}=5V		420		mΩ
Low-side switch on resistance[3]	R_{ON_LS}	V_{IN}=15V		220		mΩ
High-side switch leakage		V_{EN}=0V, V_{SW}=0V			1	μA
Low-side switch leakage		V_{EN}=0V, V_{SW}=60V			1	μA
Current limit	I_{LIM}			0.9		A
VIN UVLO rising threshold				4.3		V
VIN UVLO falling threshold				4.0		V
VIN UVLO hysteresis				0.3		V
Soft-start time	T_{SS}	V_{FB} from 10% to 90%		0.8		ms
Oscillator frequency	f_{SW}			1.5		MHz
Minimum switch on time [4]	t_{ON}			120		ns
Shutdown supply current	I_S	V_{EN}<0.3V, V_{IN}=15V		1		μA
Quiescent supply current	I_Q	No load, V_{FB}=0.83V, no switching		200		μA
Thermal shutdown [4]				150		°C
Thermal shutdown hysteresis [4]				35		°C
Enable rising threshold	V_{IH}	Low to high		1.55		V
Enable falling threshold				1.22		V
Enable threshold hysteresis				330		mV

Notes:

3) Not tested in production.

4) Not tested in production and guaranteed by over-temperature correlation. Not tested in production and derived from bench characterization

Detailed description

The ME3136 employs fixed-frequency peak-current mode control. It enters PFM mode at light load to achieve high efficiency. The device is internally compensated, which reduces design time and requires few external components. It's very low operational quiescent current makes it suitable for battery- powered applications.

Fixed Frequency Peak Current Mode Control

The ME3136 is a step-down synchronous buck converter with integrated high-side (HS) and low-side (LS) switches (synchronous rectifier). The ME3136 supplies a regulated output voltage by turning on the high-side and low-side NMOS switches with controlled duty cycle. During high-side switch ON time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current increases with a linear slope of $(V_{IN}–V_{OUT})/L$. When the high-side switch is turned off by the control logic, the low-side switch is turned on after an anti-shoot-through dead time. Inductor current discharges through the low-side switch with a slope of $–V_{OUT}/L$.

The control parameter of a buck converter is defined as Duty Cycle $D=T_{ON}/T_{OSC}$, where T_{ON} is the high-side switch ON time and T_{OSC} is the switching period. The converter control loop maintains a constant output voltage by adjusting the duty cycle D.

A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak-current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the ON time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, making designing easy and providing stable operation when using a variety of output capacitors.

Pulse-Skipping Mode (PSM)

During light load operation, PSM mode is activated to maintain high efficiency operation. When either the minimum high-side switch ON time t_{ON_MIN} or the minimum peak inductor current I_{PEAK_MIN} (300 mA typical) is reached, the switching frequency decreases to maintain regulation. In PSM mode,

switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to a significant drop in effective switching frequency.

Error Amplifier (EA)

The error amplifier is composed of an internal op-amp with an R-C feedback network connected between its output node (internal COMP node) and its negative input node (FB). When the FB voltage (V_{FB}) drops below the internal reference voltage (V_{REF}), the op-amp drives the COMP output high, producing a higher switch peak current output and delivering more energy to the output. Conversely, when VFB rises, the switch peak current output drops.

Connect FB to the tap of a voltage divider connected between VOUT and GND composed of R1 and R2. R1 also serves to control the gain of the error amplifier in addition to the internal compensation R-C network

Shutdown Control (EN)

The ME3136 has a dedicated enable control pin (EN). When VIN rises above the threshold, EN can enable or disable the chip for high effective logic. Its falling threshold is 1.22V, and its rising threshold is about 1.55V. An internal 1.7MΩ resistor from EN to GND allows EN to be float to shut down the IC.

EN is clamped internally using a 6V series Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to VIN limits the EN input current below 100μA. For example, with 12V connected to VIN, R_{PULLUP}≥(12V-5.5V) ÷100μA=65kΩ.

Connecting EN to a voltage source directly without a pull-up resistor requires limiting the amplitude of the voltage source to ≤5.5V to prevent damage to the Zener diode. This feature allows self-start-up when the input voltage is in the operating range of 4.3 V to 60 V.

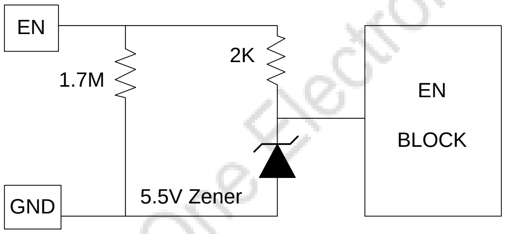


Figure4. Zener Diode between EN and GND

VIN Under-Voltage Lockout (UVLO)

The ME3136 also employs VIN undervoltage lockout protection (UVLO). If VIN voltage is below its UVLO threshold of 4.0 V, the converter is turned off.

Internal Soft Start (SS)

The integrated soft-start circuit prevents input inrush current impacting the ME3136 and the input power supply. Soft start is achieved by slowly ramping up the internal reference voltage when the device is first enabled or powered up. The typical soft-start time is 1.0mS.

Thermal Shutdown

Thermal shutdown prevents thermal runaway. When the silicon die temperature exceeds its upper threshold, the entire chip shuts down. When the temperature drops below its lower threshold, the chip is enabled again.

Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The ME3136 incorporates both peak and valley inductor current limit to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current runaway during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for sustained short circuits.

Low Dropout Operation

The ME3136 is designed to operate at almost 100% duty cycle to improve dropout. When the current in the HS-FET does not reach the COMP-set current value within one PWM cycle, the HS-FET remains on to prevent a turn-off operation. The HS-FET can remain on for a maximum of 5.5μs and then turns off for a minimum of 110ns.

Start-Up and Shutdown Circuit

If both VIN and VEN exceed their respective thresholds, the chip starts up. The reference block first starts to generate a stable reference voltage and current, and then the internal regulator starts to provide a stable supply for the rest of the circuit.

Three events can shut down the chip: EN low, VIN low, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Applications Information

Feedback Resistors

Set the output voltage of ME3136 by using a resistor divider (see Figure 3):

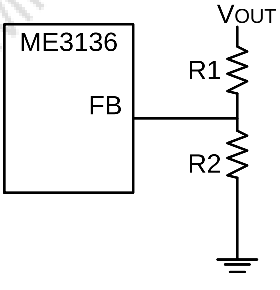


Figure5. FB Resistor Divider to Set V_{OUT}

Calculate the output voltage with Equation (1):

$$V_{OUT} = V_{FB}\frac{(R1+R2)}{R2} \quad (1)$$

The feedback resistor (R1) also sets the feedback loop bandwidth with the internal compensation network.

To achieve optimal stability performance and transient response, choose R1 to be around 150kΩ in applications with a 12V output rail. Then, calculate R2 with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V}-1} \quad (2)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection vs. Output Voltage Setting

V_{OUT}	R1	R2
12V	150kΩ (1%)	10.7kΩ (1%)
5V	56kΩ (1%)	10.7kΩ (1%)
3.3V	40.2kΩ (1%)	13kΩ (1%)

Inductor

For most applications, choose an inductance such that the inductor ripple current, ΔI_L, is between 30% and 40% of the maximum DC output current at nominal input voltage. The inductance value can be calculated with Equation (3):

$$L1 = \frac{V_{OUT}}{f_s \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (4):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_s \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Where I_{LOAD} is the load current.

Input Capacitor

The input capacitor (C1) can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, ceramic capacitor (C2) (e.g.: 0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input

The input voltage ripple caused by the capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Output Capacitor

An output capacitor (C4) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are recommended to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C4}\right) \quad (6)$$

Where L is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8\times f_S^2\times L\times C4}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR} \quad (8)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

In power meter applications, large-value capacitors are usually used as the output capacitors, typically, with an R_{ESR} and capacitance with a large variation under low temperature. This large temperature variation changes the part's feedback loop, making it difficult to keep the loop stable over the full operation temperature. So, tantalum capacitor or polymer capacitor which with better temperature stability is recommended for low- temperature applications.

Compensation Components

The goal of compensation design is to shape the converter transfer function to achieve a desirable loop gain. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies can cause system instability. Generally, set the crossover frequency to equal approximately one-tenth of the switching frequency. If using an electrolytic capacitor, select a loop bandwidth no higher than 1/4 of the ESR zero frequency (f_{ESR}), where f_{ESR} can be calculated with Equation (9):

$$f_{ESR} = \frac{1}{2\pi\times C4\times R_{ESR}} \quad (9)$$

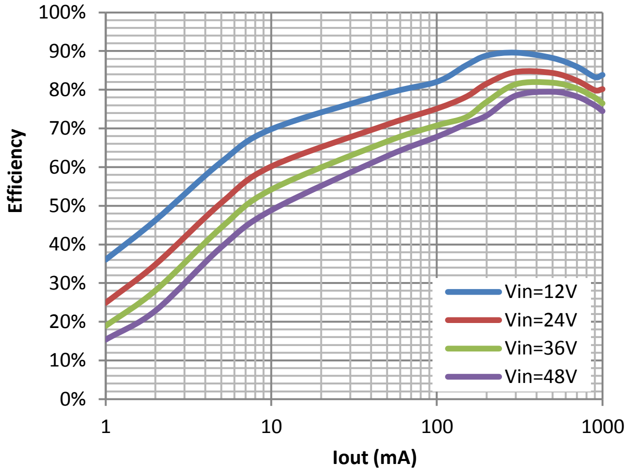
Table 3 shows a component selection guide for 12V/5V/3.3V output rail applications.

Table 3: Components Selection Guide

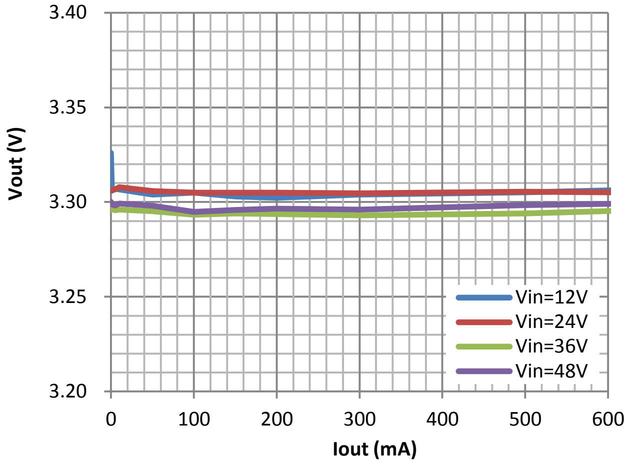
V_{OUT}	R1	R2	L1	C3	C4
12V	150kΩ (1%)	10.7kΩ (1%)	22µH	22µF	470µF
5V	56kΩ (1%)	10.7kΩ (1%)	15µH	22µF	470µF
3.3V	40.2kΩ (1%)	13kΩ (1%)	10µH	22µF	470µF

Typical Performance Characteristics

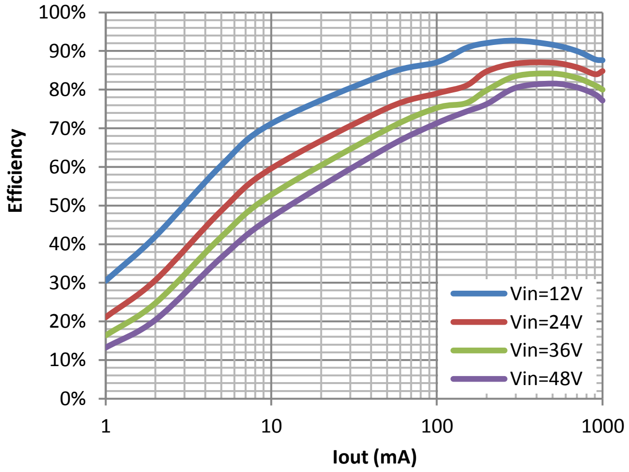
Efficiency vs. Output Current
(Vout=3.3V)



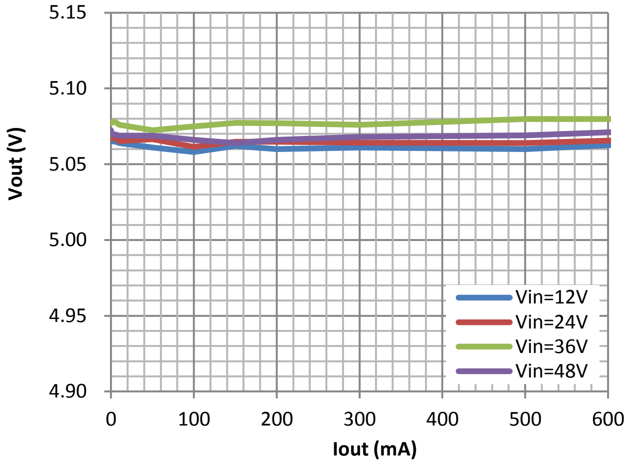
Load Regulation
(Vout=3.3V)



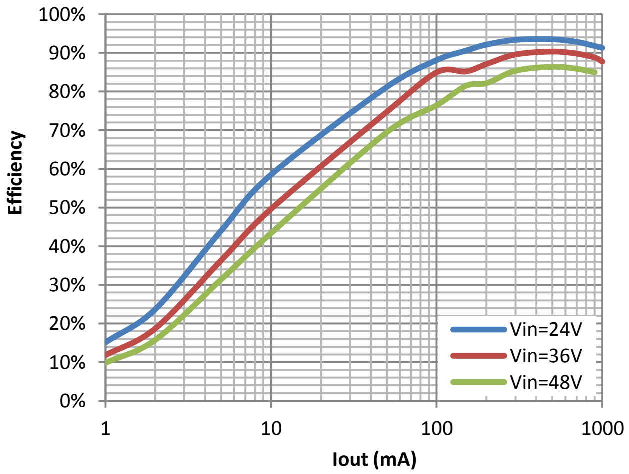
Efficiency vs. Output Current
(Vout=5V)



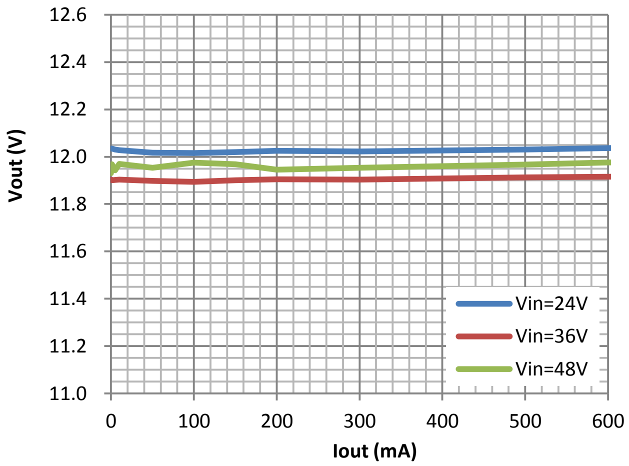
Load Regulation
(Vout=5V)



Efficiency vs. Output Current
(Vout=12V)

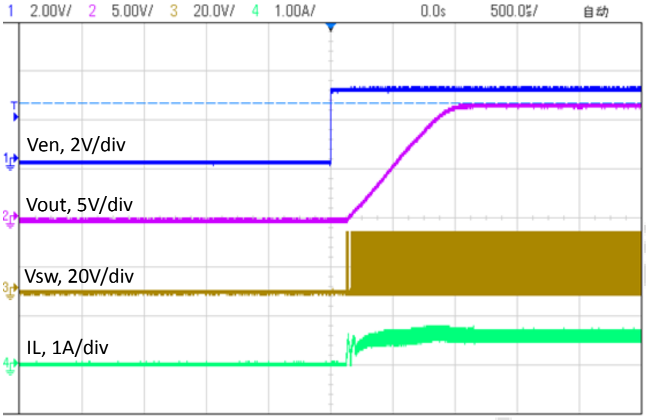


Load Regulation
(Vout=12V)



EN Power Up

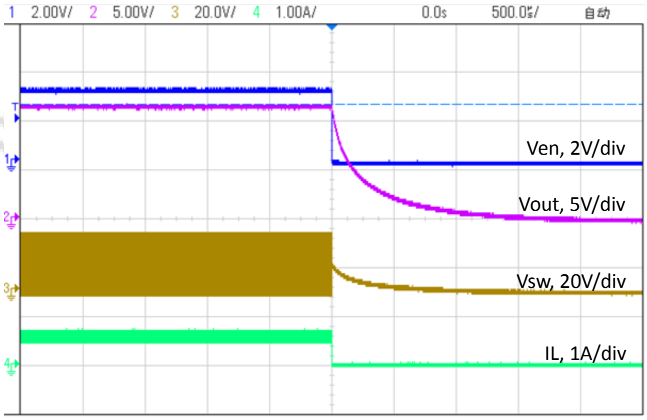
(EN=0V to 3V, Vin=24V, Vout=12V, Iout=600mA)



CH1: EN; CH2: Vout; CH3:Vsw; CH4: IL

EN Power Off

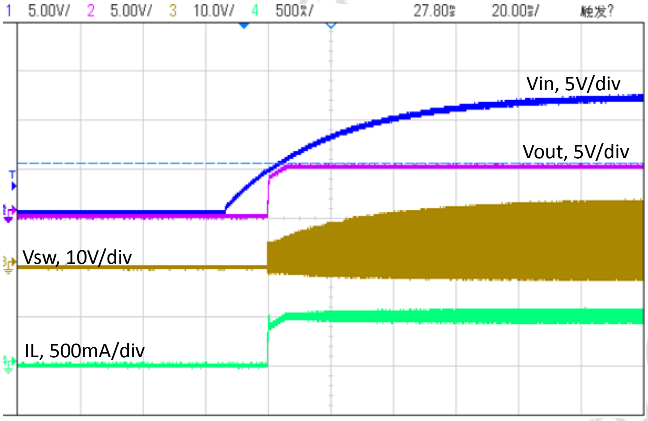
(EN=3V to 0V, Vin=24V, Vout=12V, Iout=600mA)



CH1: EN; CH2: Vout; CH3:Vsw; CH4: IL

VIN Power Up

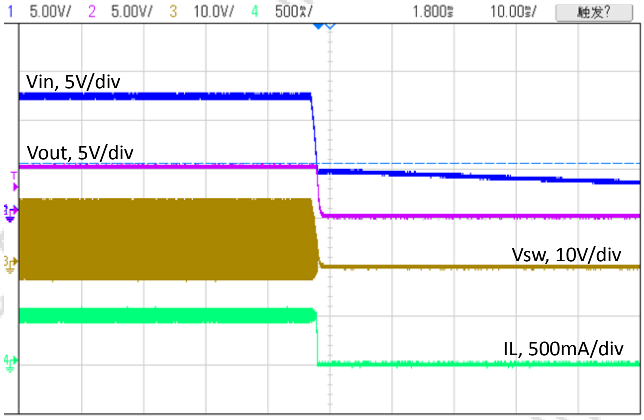
(VIN=0V to 12V, Vout=5V, Iout=600mA)



CH1: Vin; CH2: Vout; CH3:Vsw; CH4: IL

VIN Power Off

(VIN=12V to 0V, Vout=5V, Iout=600mA)

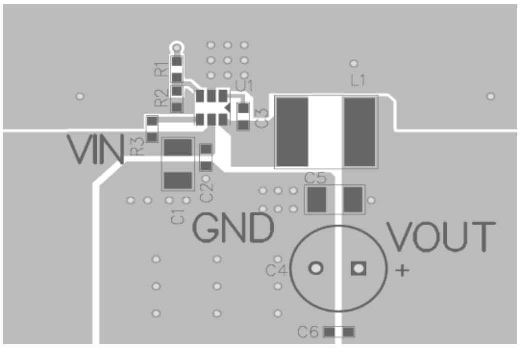


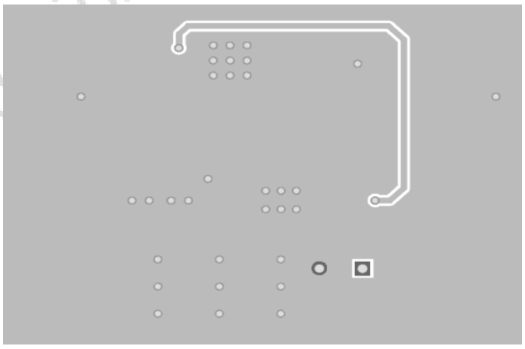
CH1: Vin; CH2: Vout; CH3:Vsw; CH4: IL

PCB Layout Guidelines

Proper PCB design and layout is important in a high-current, fast-switching circuits (with high voltage slew rate) to assure appropriate device operation and design robustness. As expected, certain issues must be considered before designing a PCB layout using the ME3136.

The below shows an example PCB layout based on those well-known guidelines.



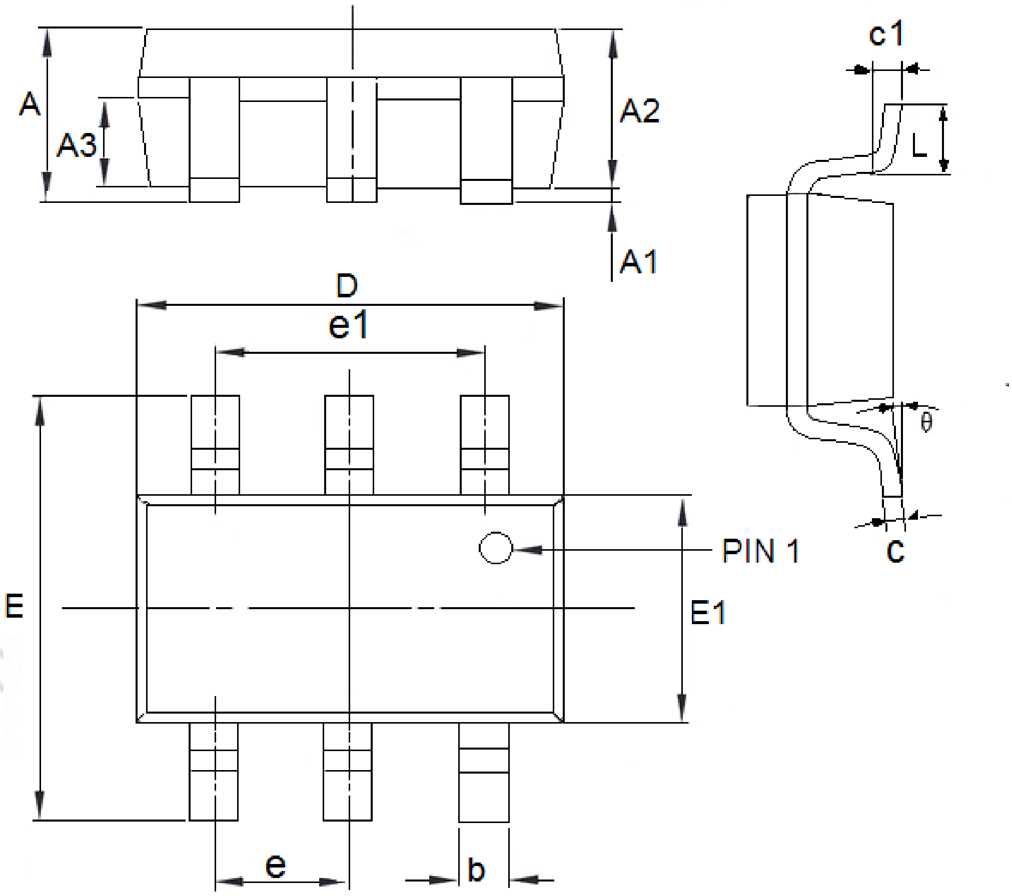


Package Quantity

Package Type	Minimum Packing QTY	UNITS	Small Box	Large BOX
SOT23-6	3000	Tape & Reel	30K	120K

Package Information

- **Package Type: SOT23-6**



DIM	Millimeters		Inches	
	Min	**Max**	**Min**	**Max**
A	1.05	1.45	0.0413	0.0571
A1	0	0.15	0.0000	0.0059
A2	0.9	1.3	0.0354	0.0512
A3	0.55	0.75	0.0217	0.0295
b	0.25	0.5	0.0098	0.0197
c	0.1	0.25	0.0039	0.0098
D	2.7	3.12	0.1063	0.1228
e1	1.9(TYP)		0.0748(TYP)	
E	2.6	3.1	0.1024	0.1220
E1	1.4	1.8	0.0551	0.0709
e	0.95(TYP)		0.0374(TYP)	
L	0.25	0.6	0.0098	0.0236
θ	0	8°	0.0000	8°
c1	0.2(TYP)		0.0079(TYP)	

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