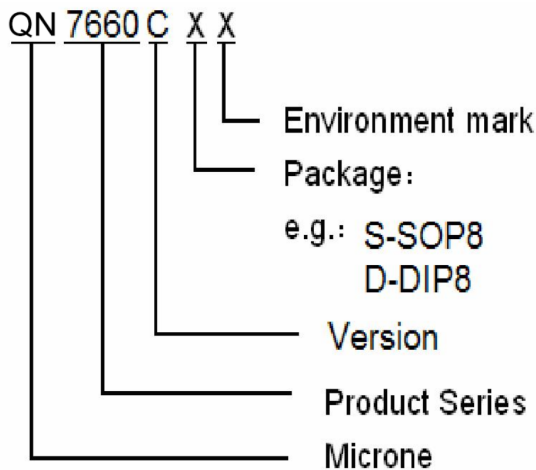


QN7660C Charge Pump DC-DC Voltage Converter

QN7660C is a charge pump dc-to-dc voltage converter using AL-gate CMOS technology and optimization design. It converts a +2.5V to +10V input to a corresponding -2.5V to -10V output using only two external capacitors, eliminating inductors and their associated cost, size and EMI. The on-board oscillator operates at a nominal frequency of 10KHz. Operation below 10 KHz (for lower supply current applications) is possible by connecting an external capacitor from OSC to ground.

Selection Guide



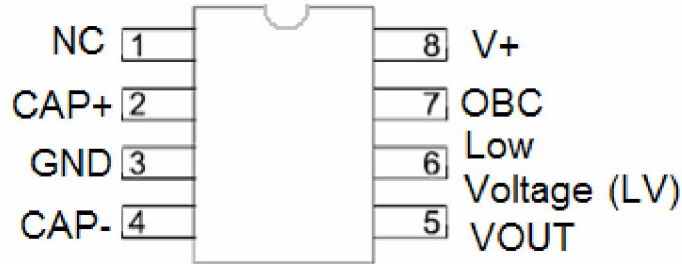
Features

- Converts +5V Logic supply to $\pm 5V$;
- Wide input voltage range: 2.5V~10V ;
- Efficient voltage conversion: 99.9% ;
- Good power efficiency: 98% ;
- Low power supply: 40uA @5V input ;
- Easy to use: only two external capacitors required ;
- Compatible with RS232 negative powersupply standard ;
- High ESD protection: up to 3kV ;
- No Dx diode needed for high voltage operation ;
- Package : SOP8, DIP8.

Applications

- LCD Display Module ;
- Specially designed LCD display module ;
- Instrument product.

Pin Configuration

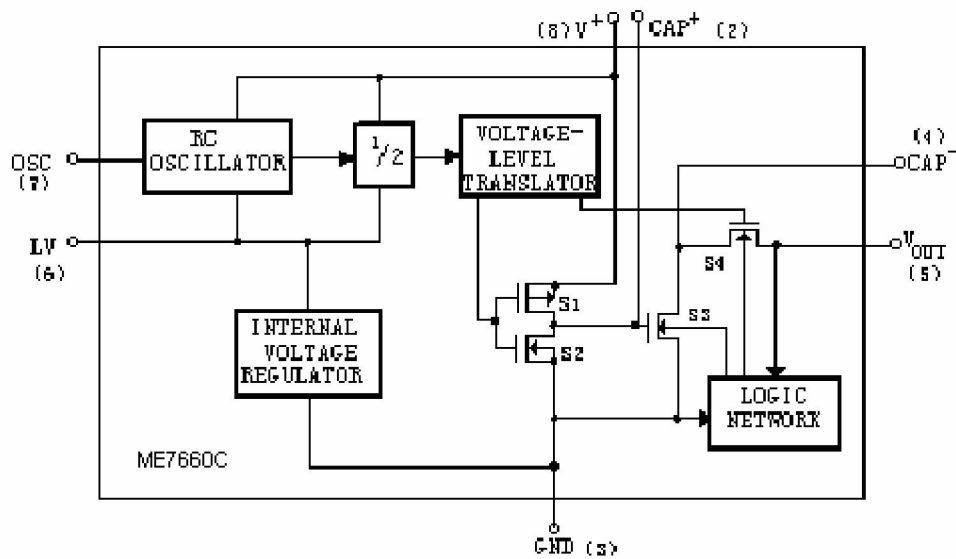


Pin Assignment

QN7660C

PIN Number		PIN NAME	FUNCTION
SOP8	DIP8		
1	1	NC	No connection
2	2	CAP ⁺	Connecting external capacitor(+) pin
3	3	GND	Ground pin
4	4	CAP ⁻	Connecting external capacitor(-) pin
5	5	Vout	Voltage output pin
6	6	Low Voltage	Low voltage selection pin
7	7	OSC	Connecting oscillation capacitor pin
8	8	V ⁺	Power supply pin

Block Diagram



Block of function module in chip

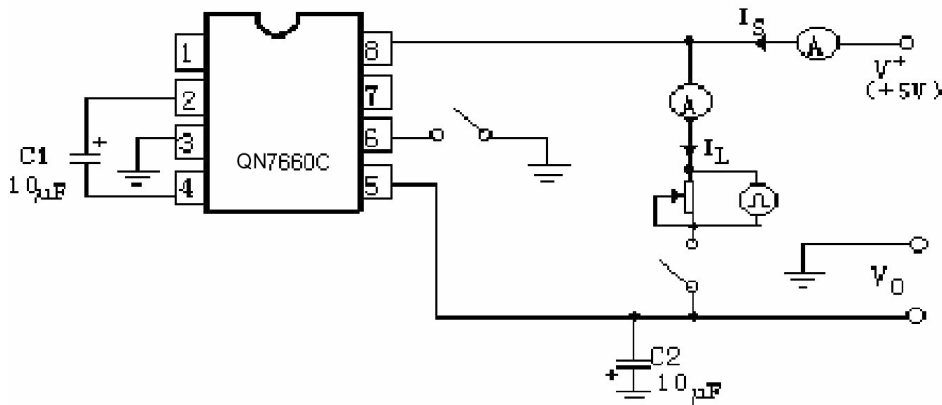
Absolute Maximum Ratings

PARAMETER		SYMBOL	RATINGS	UNITS
Input voltage		V_{IN}	+10.5V	V
LV PIN input voltage		V_{LX}	-0.3 ~ ($V^+ + 0.3$) (if $V^+ < 5.5V$) ($V^+ - 5.5V$) ~ ($V^+ + 0.3V$) (if $V^+ > 5.5V$)	V
OSC PIN input voltage		V_{OSC}		
LV PIN input current		I_{LV}	20 (if $V^+ > 3.5V$)	μA
Output Short Duration ($V_{supply} = 5.5V$)				
Continuous Total Power Dissipation ($T_A = 75^\circ C$)	SOP8	P_d	470	mW
	DIP8	P_d	730	mW
Operating Ambient Temperature		T_{Opr}	-40 ~ +85	
Storage Temperature		T_{stg}	-65 ~ +150	
Soldering temperature and time		T_{solder}	260 , 10s	

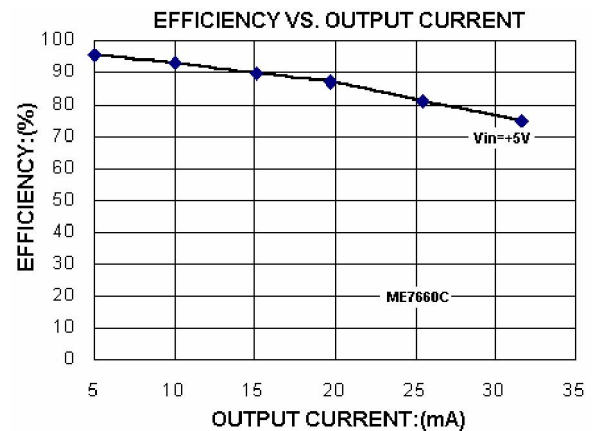
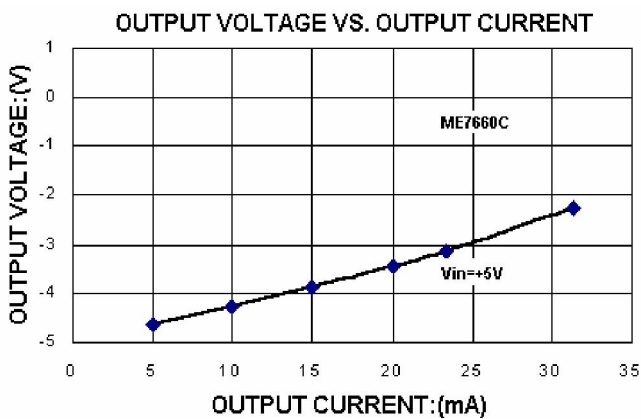
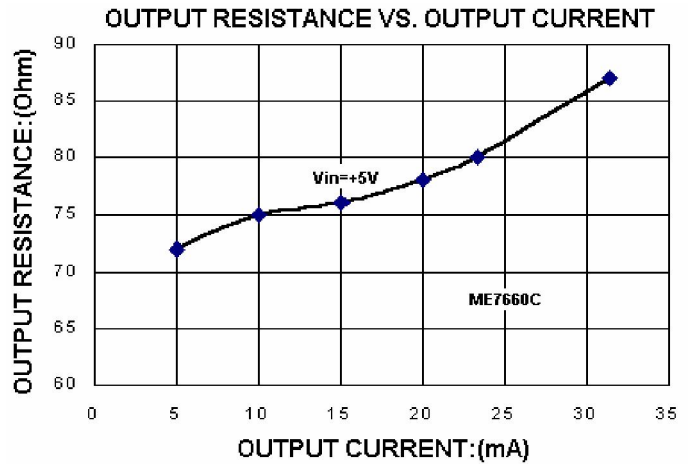
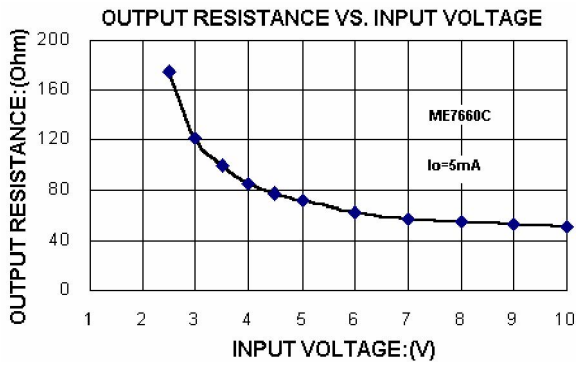
Electrical Characteristics ($V^+ = 5V, C_{OSC} = 0$)

Symbol	Item	Conditions	Min	Typ	Max	Unit
I^+	Supply Current	$R_L = \infty$	—	40	100	μA
V^+_H	Supply Voltage, High	LV Open	3.5	—	10	V
V^+_L	Supply Voltage, Low	LV to GND	2.5	—	3.5	V
R_{OUT}	Output Resistance	$I_{OUT} = 20mA$ $T_A = 25^\circ C$		70		
		$I_{OUT} = 5mA$ $V^+ = 3V$ $T_A = 25^\circ C$		120		
F_{OSC}	Oscillator Frequency	Pin 7 open	—	10	—	kHz
P_{EFF}	Power Efficiency	$R_L = 5k\Omega$	95	98	—	%
$V_{OUT} E_{FF}$	Voltage Conversion Efficiency	$R_L = \infty$	98	99.9	—	%

Test Circuits



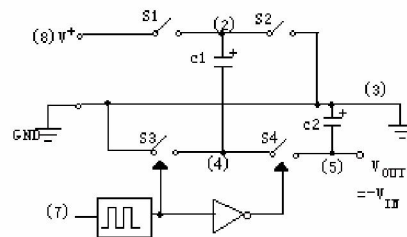
Type Characteristics



Operation

QN7660C together with two external capacitors C1, C2 complement a voltage Inverter. Capacitor C1 is charged to a voltage V^+ , for the first half cycle when switches S1 and S3 are closed (while switches S2 and S4 are open during this half cycle); During the second half cycle of operation, switches S2 and S4 are closed, with S1 and S3 open, thereby shifting capacitor C2 negatively to $-V^+$.

The voltage regulator portion of the chip is an integral part of the anti-latch-up circuitry. Its inherent voltage drop can degrade operation at low voltages. To improve low-voltage operation, the LV pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure latch-up-proof operation.



Charge Pump Voltage Converter operating process

Theoretical Power Efficiency Considerations

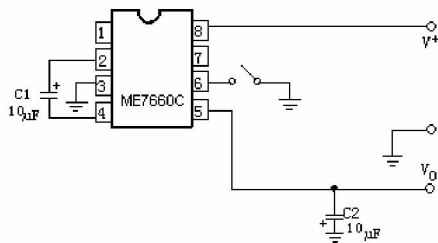
In theory, a capacitive charge pump can approach 100% efficiency if certain conditions are met:

- 1、 The drive circuitry consumes no power.
- 2、 The output switches have extremely low ON resistance and no offset when operation.
- 3、 The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

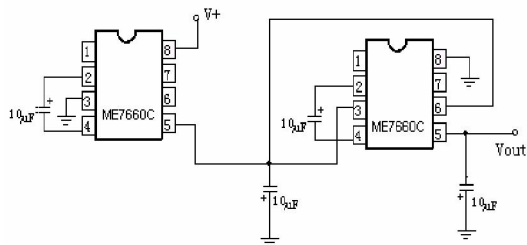
Notes:

- 1、 Supply voltage should not exceed maximum rating;
- 2、 Do not connect LV terminal to GND for supply voltages greater than 3.5V;
- 3、 Do not short circuit the output to V⁺ supply for voltages above 5.5V for extended periods;
- 4、 Polarized capacitors should be connected as the figure above.

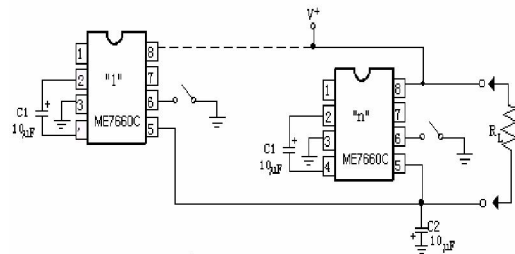
Typical Application



Above figure is the basic application circuit to provide a negative supply from -2.5V~ -10V while a positive supply from +2.5V ~ +10V is available. When V⁺=+5V, the output resistance is about 70 Ω; The output voltage is -4V while the load current is 10mA.

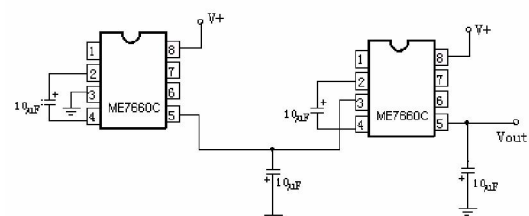


QN7660C may be cascaded as shown above to produce larger negative output voltage (-10V). However, The output resistance is approximately two of a single chip resistance.

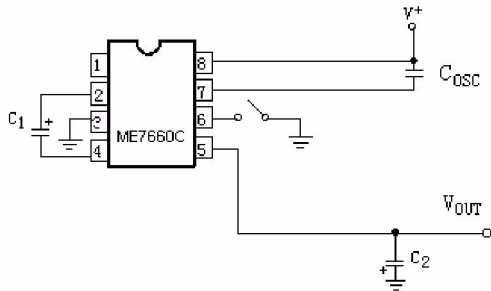


QN7660C may be paralleled to reduce output resistance (see the above figure)

$$R_{out} = R_{out}(\text{of QN7660C}) / n(\text{number of devices})$$

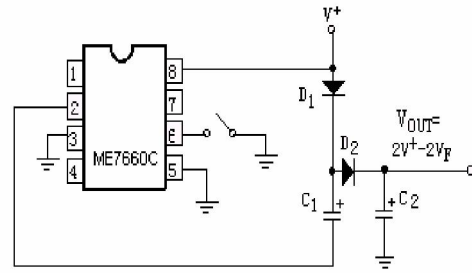


QN7660C may be cascaded as shown above to produce larger negative output voltage (-15V). However, The output resistance is approximately two of a single chip resistance.

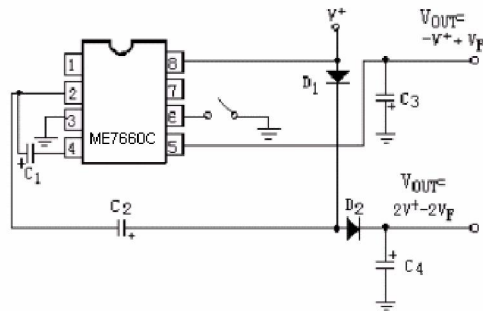


To increase the conversion efficiency, the oscillator frequency may be lowered by connecting a capacitor from pin 7 and pin 8 as shown above.

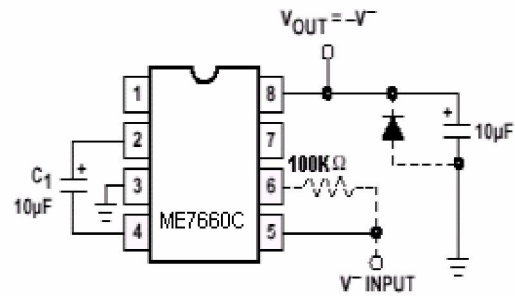
This reduces the switching losses. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump and reservoir capacitors. So, the values of C1 and C2 should be increased by the same factor that the



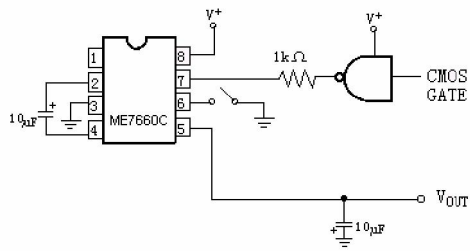
QN7660C may be applied to achieve positive voltage multiplication using the circuit shown in the above figure



In above figure, C1, C3 are the pump and reservoir capacitors respectively for the generation of the negative voltage; C2, C4 are the pump and reservoir capacitors respectively for the multiplied positive voltage. When +5V supply is provided, +9V and -5V can be generated.



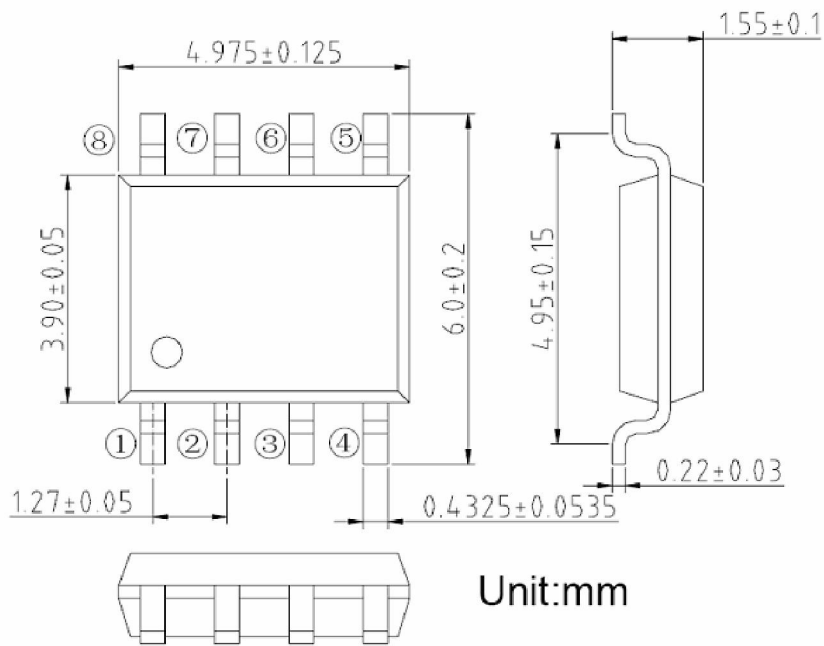
Since the switches that allow the charge pumping operation are bi-directional, the charge transfer can be performed backwards as easily as forwards. In the above figure, QN7660C transforming -5V to +5V. The only problem here is that the internal clock and switch-drive section will not operate until some positive voltage has been generated. An initial inefficient pump, as shown in left figure, could be used to start this circuit up, after which it will bypass the other (D1 and D2 in left figure would never turn on), or else the diode and resistor shown dotted in above figure can be used to "force" the internal regulator on.



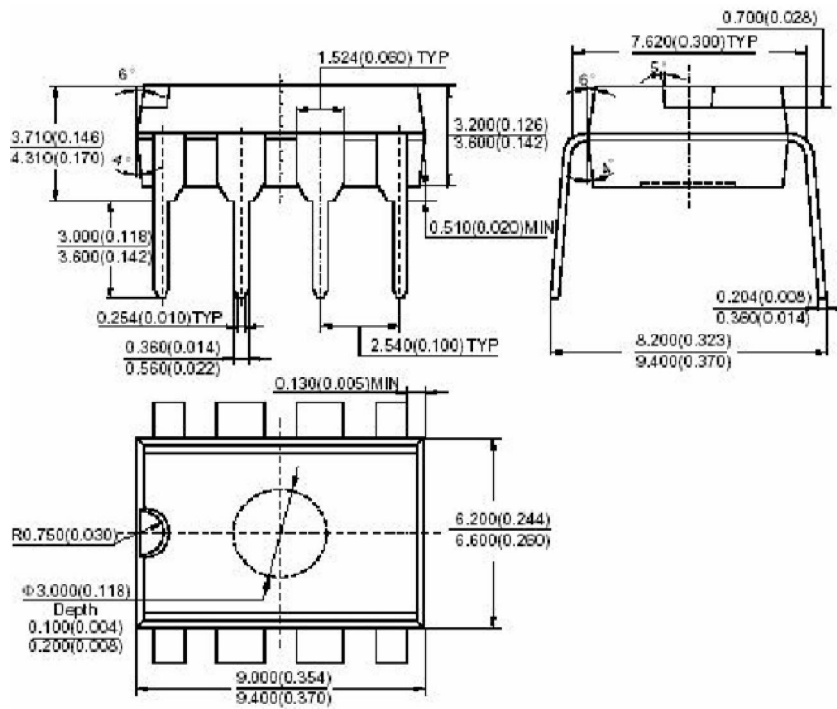
In some applications due to noise, it may be desirable to increase the oscillator frequency. This can be achieved by overdriving the oscillator from an external clock as shown in the above figure. The external clock output should connect a 1k resistor to prevent device latch-up. Besides, the pump frequency will be half of the clock frequency because of the internal circuit

Package Diomensions

SOP8



DIP8



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